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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/981,484	CALLWAY, EDWARD G.	
	Examiner	Art Unit	
	JONI HSU	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-22 and 29-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29* is/are allowed.

6)☒ Claim(s) *19,21,22 and 30-39* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed September 15, 2008 have been fully considered but they are not persuasive.

2. As per Claim 19, Applicant argues that the Office Action fails to pinpoint which section of Taylor (US006118461A) purports to teach second rendered frame is output immediately after first rendered frame has been output, and thus teaches second signal corresponds to alternating frame of video. Taylor's system sequentially maps the subsystems in a given chain in order to completely map through each of the display units 103 and the system memory system 108 instead of generating a second signal at a second device…wherein the second signal corresponds to an alternating frame of video. Taylor is directed to a system wherein each display control unit controls display data of a respective region of a single screen of a display device. An adjacent frame as taught by Taylor can not be an alternating frame of video (p. 6-7).

In reply, the Examiner points out that Claim 19 does not specify that the frame must be an entire frame. As per Claim 30, Taylor is used to modify Walls (US006215486B1), and this combination teaches the claimed limitation. Taylor teaches frame from frame buffer of display control unit 103a (c. 5, ll. 65-c. 6, ll. 1) is output first to display (110) (c. 6, ll. 50-61), then frame from frame buffer of display control unit 103b (c. 5, ll. 65-c. 6, ll. 1) is output next to display (c. 7, ll. 11-30). While the data in the frame buffer 105 of one selected unit 103 is being updated, the remaining units 103 can continue to raster out data and refresh their corresponding data (c. 5, ll. 65-c. 6, ll. 1). Since the frame buffers of the units are being updated sequentially (c. 5, ll. 65-67; c. 6, ll. 1, 50-61; c. 7, ll. 11-30), this means that while the second frame buffer is being updated,

the first frame buffer is outputting a first rendered frame, and after the second frame buffer is finished being updated, the first frame buffer is then updated while the second frame buffer outputs a second rendered frame. Therefore, Taylor teaches second rendered frame is output immediately after first rendered frame has been output, and thus teaches second graphics device operative to render second alternating frame of video. Taylor is used to modify Walls, and since Walls teaches portion of "logical frame" is entire frame of video (c. 1, ll. 28-31, 37-42; c. 2, ll. 19-26, 39-41), device of Walls can be modified so portions of "logical frame" that are entire frames of video are alternating frames of video, as suggested by Taylor.

3. Applicant argues that the cited references do not teach adjusting the second device until a value of the second signal at the first output node substantially matches the determined value of the first signal at the first output node (p. 8).

In reply, the Examiner points out that Gonsalves (US006847272B1) teaches making color modifications to correct color errors due to process errors (c. 1, ll. 26-29). Such corrections include matching colors and tones from shot to shot (c. 1, ll. 34-38). Gonsalves teaches adjusting values of selected destination color component for color matching (c. 3, ll. 42-50; c. 24, ll. 16-19). So, combining Taylor and Gonsalves, it would be obvious to adjust 2nd device until value of 2nd signal representing color component data at 1st output node substantially matches determined value of 1st signal representing color component data at 1st output node.

4. Applicant argues that Claim 30 as amended includes substantially similar limitations to those described in allowed Claim 29 (p. 8).

In reply, the Examiner points out that Claim 29 is still much more detailed than Claim 30. For instance, Claim 29 has additional limitations that second video output port is coupled to first

video component output of second graphics device, and rendering entire temporally adjacent frame of video. It is because of these additional limitations of Claim 29 that Claim 29 is allowable. As per Claim 30, Lengyel (US006016150A) teaches compositor (60, Fig. 2) is operatively coupled to receive rendered video (50, 52; c. 8, ll. 30) from any of multiple graphics devices and combines input rendered video and outputs it to first video output port (196, Fig. 17) in order to ensure inputs to compositing operation are synchronized (c. 8, ll. 55-60; c. 24, ll. 7-13, 22-27). So, by implementing this compositor taught by Lengyel into the combination of Walls and Taylor, the combination can be modified to include a common port operatively coupled to the first graphics device and the second graphics device, the common port being operative to receive the first and second frames of rendered video from either of the first and second graphics devices. Therefore, the combination of Walls, Lengyel, and Taylor still teaches the limitations of Claim 30.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US006118461A) and Gonsalves (US006847272B1).

Taylor teaches method of providing video signal, method comprising generating 1st signal at 1st device (103a, Fig. 1; c. 4, ll. 14-21, 52-57), wherein 1st signal is representative of 1st video output component (c. 5, ll. 65-c. 6, ll. 1); providing 1st signal to 1st node (109); determining value of 1st signal at 1st output node (c. 5, ll. 1-3); generating 2nd signal at 2nd device (103b), wherein 2nd signal is representative of 1st video output component (c. 4, ll. 52-57). Frame from frame buffer of display control unit 103a (c. 5, ll. 65-c. 6, ll. 1) is output 1st to display (110) (c. 6, ll. 50-61), then frame from frame buffer of display control unit 103b (c. 5, ll. 65-c. 6, ll. 1) is output next to display (c. 7, ll. 11-30). While the data in the frame buffer 105 of one selected unit 103 is being updated, the remaining units 103 can continue to raster out data and refresh their corresponding data (c. 5, ll. 65-c. 6, ll. 1). Since the frame buffers of the units are being updated sequentially (c. 5, ll. 65-67; c. 6, ll. 1, 50-61; c. 7, ll. 11-30), this means that while the second frame buffer is being updated, the first frame buffer is outputting a first rendered frame, and after the second frame buffer is finished being updated, the first frame buffer is then updated while the second frame buffer outputs a second rendered frame. Therefore, Taylor teaches second rendered frame is output immediately after first rendered frame has been output, and thus teaches 2nd signal corresponds to alternating frame of video. Taylor teaches providing 2nd signal of 2nd device to 1st output node (c. 5, ll. 1-3). Since digital to analog converter receives digital data (1st signal) from controller 104 (first output node) and outputs analog data to drive display in response to 1st signal from 1st output node (c. 5, ll. 1-3), it must inherently determine value of 1st

signal in order to output analog data, since it outputs analog data in response to 1st signal. This means determined value of 1st signal causes digital to analog converter to output analog data.

But, Taylor does not teach adjusting 2nd device until value of 2nd signal representing color component information at 1st output node substantially matches determined value of 1st signal representing color component data at 1st output node. But, Gonsalves teaches making color modifications to correct color errors due to process errors (c. 1, ll. 26-29). Such corrections include matching colors and tones from shot to shot (c. 1, ll. 34-38). Gonsalves teaches adjusting values of selected destination color component for color matching (c. 3, ll. 42-50; c. 24, ll. 16-19). So, combining Taylor and Gonsalves, it would be obvious to adjust 2nd device until value of 2nd signal representing color component data at 1st output node substantially matches determined value of 1st signal representing color component data at 1st output node.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Taylor to include adjusting 2nd device until a value of 2nd signal representing color component information at first output node substantially matches determined value of first signal representing color component information at first output node because Gonsalves teaches this corrects color errors due to process errors (c. 1, ll. 26-29).

8. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US006118461A) and Gonsalves (US006847272B1) in view of Deering (US005963200A).

9. As per Claim 21, Taylor and Gonsalves are relied on for teachings relative to Claim 19.

However, Taylor and Gonsalves do not explicitly teach value of 1st and 2nd signals is voltage value. But, Deering teaches adjusting the 2nd device (14) until a value of 2nd signal at 1st

output node substantially matches the determined value of the 1st signal at the 1st output node (c. 3, 19-25; c. 5, ll. 22-45), and value of 1st and 2nd signals is voltage value (c. 1, ll. 61-c. 2, ll. 2).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Taylor and Gonsalves so value of 1st and 2nd signals is voltage value because Deering suggests it is well-known in the art video output is controlled by voltage levels (c. 1, ll. 61-c. 2, ll. 2).

10. As per Claim 22, Taylor does not teach step of determining includes modifying and comparing value of first signal until value of first signal substantially matches predetermined value. However, Deering teaches this limitation (c. 5, ll. 22-45).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Taylor to include step of determining includes modifying and comparing value of first signal until value of first signal substantially matches predetermined value because Deering suggests advantage that master provides single timing reference (c. 5, ll. 22-45). System utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in viewed images because computers do not operate from single timing reference (c. 3, ll. 12-18). So, because master provides single timing reference, this method avoids exhibiting aberrations in the viewed images.

11. Claims 30, 31, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1), Lengyel (US006016150A), and Taylor (US006118461A).

12. As per Claim 30, Walls teaches multiple graphics devices (202, 204, 206, 208, Fig. 2), each operable to render video for entire screen for one display device that displays portion of complete composite display, such that combination of all display devices present illusion of one

large logical screen that displays complete composite display (c. 1, ll. 28-31, 37-42; c. 2, ll. 19-26, 39-41). Since each graphics device is operable to render video for entire screen for one display device (c. 2, ll. 39-41), each graphics device is considered to render entire frame of video. So, Walls teaches apparatus for providing video signals having 1st graphics device 202 to render entire 1st frame of video; and 2nd graphics device 204 to render entire 2nd frame of video.

But, Walls does not teach common port operatively coupled to the first graphics device and the second graphics device, the common port being operative to receive 1st and 2nd frames of rendered video from either of 1st and 2nd graphics devices. But, Lengyel teaches 1st graphics device (56, Fig. 2) operative to render 1st portion (46) of complete composite display (34); and 2nd graphics device (58) operative to render second portion (48) of complete composite display (c. 7, ll. 13-16, 66-67; c. 8, ll. 1-2). Compositor (60) is operatively coupled to receive rendered video (50, 52; c. 8, ll. 30) from any of multiple graphics device and combines input rendered video and outputs it to common port (196, Fig. 17) in order to ensure inputs to compositing operation are synchronized (c. 8, ll. 55-60; c. 24, ll. 7-13, 22-27). So, common port is operatively coupled to receive rendered video from any of graphics devices. So, by implementing this compositor taught by Lengyel into Walls, Walls can be modified so common port is operatively coupled to the first graphics device and the second graphics device, the common port being operative to receive 1st and 2nd frames of rendered video from either of 1st and 2nd graphics devices in order to ensure inputs to compositing operation are synchronized so output of complete composite display is synchronized. This would be obvious for reasons for Claim 29.

However, Walls and Lengyel do not expressly teach second graphics device renders alternating frame of video. However, Taylor teaches frame from frame buffer of display control

unit 103a (c. 5, ll. 65-c. 6, ll. 1) is output first to display (110) (c. 6, ll. 50-61), then frame from frame buffer of display control unit 103b (c. 5, ll. 65-c. 6, ll. 1) is output next to display (c. 7, ll. 11-30). While the data in the frame buffer 105 of one selected unit 103 is being updated, the remaining units 103 can continue to raster out data and refresh their corresponding data (c. 5, ll. 65-c. 6, ll. 1). Since the frame buffers of the units are being updated sequentially (c. 5, ll. 65-67; c. 6, ll. 1, 50-61; c. 7, ll. 11-30), this means that while the second frame buffer is being updated, the first frame buffer is outputting a first rendered frame, and after the second frame buffer is finished being updated, the first frame buffer is then updated while the second frame buffer outputs a second rendered frame. Therefore, Taylor teaches second rendered frame is output immediately after first rendered frame has been output, and thus teaches second graphics device operative to render second alternating frame of video. Taylor is used to modify Walls, and since Walls teaches portion of "logical frame" is entire frame of video, device of Walls can be modified so portions of "logical frame" that are entire frames of video are alternating frames of video, as suggested by Taylor.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Walls, Lengyel so 2nd graphics device renders alternating frame of video because Taylor suggests since 1st and 2nd rendered frames are provided to common port (109; c. 5, ll. 1-3 in Taylor), as is also taught in Lengyel as discussed above, this means only 1 rendered frame can be output to common port at a time, and so 1st rendered frame is output 1st, then 2nd rendered frame is output immediately after 1st rendered frame has been output (c. 2, ll. 58-c. 3, ll. 15; c. 6, ll. 50-61; c. 7, ll. 11-30), so 1st and 2nd rendered frames are alternating frames.

13. As per Claim 31, Walls does not teach 1st frame buffer coupled to 1st graphics device and 2nd frame buffer coupled to 2nd graphics device. But, Taylor teaches multiple graphics devices (103, Fig. 1), each operable to render video for portion of complete composite display (c. 4, ll. 14-21, 52-57; c. 5, ll. 65-c. 6, ll. 1). 1st frame buffer is operatively coupled to 1st graphics device and 2nd frame buffer is operatively coupled to 2nd graphics device (c. 4, ll. 14-18, c. 4, ll. 19-21).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Walls to include 1st frame buffer operatively coupled to 1st graphics device and 2nd frame buffer operatively coupled to 2nd graphics device because Taylor suggests while images are in process of being drawn and are not yet ready to be displayed, frame buffer can store graphics data defining color/gray-shade of each pixel of entire display frame, so when image is ready to be displayed, pixel data can immediately be retrieved out of frame buffer as corresponding display pixels on display screen are being generated (c. 1, ll. 40-46).

14. As per Claim 38, Walls and Lengyel do not explicitly teach 1st graphics device and 2nd graphics devices are video graphics adapters. However, Taylor teaches first graphics device and second graphics devices (c. 4, ll. 14-18) are video graphics adapters (c. 4, ll. 19-20, c. 4, ll. 49).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Walls and Lengyel so first graphics device and second graphics devices are video graphics adapters because Taylor suggests video graphics adapters are well-known type of graphics device (c. 1, ll. 32-39; c. 4, ll. 46-50). Majority of manufacturers have conformed to VGA graphical standard, making it the lowest common denominator that all PC graphics hardware supports. So, majority of PC graphics hardware would have video graphics adapters, and therefore video graphics adapters are well-known in the art and widely used.

15. As per Claim 39, Walls and Lengyel do not explicitly teach 1st and 2nd rendered frames are adjacent frames of video. But, Taylor teaches frame from frame buffer of display control unit 103a (c. 5, ll. 65-c. 6, ll. 1) is output 1st to display (110) (c. 6, ll. 50-61), then frame from frame buffer of display control unit 103b (c. 5, ll. 65-c. 6, ll. 1) is output next to display (c. 7, ll. 11-30). So, Taylor teaches 1st and 2nd rendered frames are adjacent frames of video. Since Claim 39 does not specify what phrase "adjacent frames of video" means, phrase "adjacent frames of video" is taken to mean that 2nd rendered frame is output immediately after first rendered frame has been output, which is what Taylor teaches. This would be obvious for reasons for Claim 29.

16. Claims 32-34, 36, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1), Lengyel (US006016150A), and Taylor (US006118461A) in view of Deering (US005963200A).

17. As per Claim 32, Walls, Lengyel, and Taylor are relied upon for teachings for Claim 31.

However, Walls does not explicitly teach at least one digital to analog converter operatively coupled to output video. However, Lengyel teaches at least one digital to analog converter (244, Fig. 19) operatively coupled to output video (c. 30, ll. 39-48).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Walls to include at least one digital to analog converter operatively coupled to output video because Lengyel suggests digital to analog converters are well-known in the art (c. 30, ll. 39-48). Video signals from digital source, such as computer, must be converted to analog form if they are to be displayed on an analog monitor, and therefore a digital to analog converter is needed. Digital to analog converters are well-known in the art and widely used.

However, Walls, Lengyel, and Taylor do not teach having voltage adjusted in order to correlate video out voltages being provided by at least one of graphics devices. However, Deering teaches 1st graphics device (14, Fig. 2) acts as master to 2nd graphics device (14) and adjusting 2nd device until value of 2nd signal at 1st output node substantially matches determined value of 1st signal at 1st output node in order to correlate video out being provided by at least one of graphics devices (c. 3, ll. 19-25; c. 5, ll. 22-45). Deering teaches value of 1st and 2nd signals is voltage value (c. 1, ll. 61-c. 2, ll. 2). This would be obvious for reasons given for Claims 21-22.

18. As per Claim 33, Walls does not teach circuitry operative to provide digital to analog conversion voltage equalization associated with 1st and 2nd graphics devices. But, Deering teaches apparatus for providing video signals having 1st graphics device (14, Fig. 2) operative to render 1st frame of video and 2nd graphics device (14) operative to render 2nd frame of video. Deering teaches circuitry operative to provide digital to analog conversion frequency equalization (c. 5, ll. 12-16). Frequencies produced by RAMDACs will vary within range of values which depends on voltage (c. 4, ll. 57-63). Adjusting frequency means adjusting voltage. This is well-known in the art, and can be found in many publications, such as Wunner (US005095280A) (c. 8, ll. 1-14). So, Deering teaches circuitry operative to provide digital to analog conversion voltage equalization.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify Walls to include circuitry operative to provide digital to analog conversion voltage equalization associated with first and second graphics devices because Deering suggests system utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in viewed images because computers do not

operate from single timing reference (c. 3, ll. 12-18). So, it is advantageous to include circuitry operative to provide digital to analog conversion frequency or voltage equalization because it avoids exhibiting aberrations in viewed images.

19. As per Claim 34, Walls does not explicitly teach outputting video from second graphics device to common port. However, Lengyel teaches this, as discussed in rejection for Claim 30.

But, Walls, Lengyel do not teach 1st graphics device includes controller to select video from 2nd graphics device to be output. But, Deering teaches master graphics device and slave graphics device (c. 5, ll. 22-25). Master graphics device emits FIELD signal and slave graphics device receives it (c. 5, ll. 25-27). Slave graphics device responds to received FIELD signal by resetting counters which produce video timing signals (c. 5, ll. 30-33). So, Deering teaches 1st graphics device includes controller to select video from 2nd graphics device to be output.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Walls and Lengyel so first graphics device includes controller operative to select video from second graphics device to be output because Deering suggests this is how master-slave system works (c. 5, ll. 22-33). Deering suggests master-slave system is advantageous because master provides single timing reference (c. 5, ll. 22-45). System utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in viewed images because computers do not operate from single timing reference (c. 3, ll. 12-18). So, because master provides single timing reference, this method avoids exhibiting aberrations in viewed images.

20. As per Claim 36, Walls and Lengyel do not teach first graphics devices acts as master to second graphics device and provides synchronization control for second graphics device. But,

Deering teaches first graphics device (14, Fig. 2) acts as master to second graphics device (14) and provides synchronization control for second graphics device (c. 3, ll. 19-25; c. 5, ll. 22-45).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify Walls and Lengyel so first graphics devices acts as master to second graphics device and provides synchronization control for second graphics device because Deering suggests master provides single timing reference (c. 5, ll. 22-45). System utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in viewed images because computers do not operate from single timing reference (c. 3, ll. 12-18). So, because master provides single timing reference, this method avoids exhibiting aberrations in the viewed images.

21. As per Claim 37, Walls and Lengyel do not teach 1st graphics device includes reference signal generator for 2nd graphics controller. But, Deering teaches 1st graphics devices includes reference signal generator for 2nd graphics controller (c. 5, ll. 22-45), as discussed for Claim 36.

22. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1), Lengyel (US006016150A), and Taylor (US006118461A) in view of Eichenberger (see citation below).

Walls, Lengyel, and Taylor are relied upon for teachings discussed relative to Claim 30.

However, Walls, Lengyel, and Taylor do not teach load operatively couplable to either one of first and second graphics devices when at least one of the first and second graphics devices is not driving common port. But, Eichenberger teaches use of dummy switch with load coupled to it for charge cancellation of active switch (pp. 257, 260). In other words, the switch that is not active or is not driving common port acts as dummy switch and has load coupled to it.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify Walls, Lengyel, Taylor to include load couplable to either one of 1st and 2nd graphics devices when one of 1st and 2nd graphics devices is not driving common port because Eichenberger suggests this reduces charge injection by charge cancellation (p. 257). Advantages of using dummy switches is well-known in the art and can be found in many publications.

Allowable Subject Matter

23. Claim 29 is allowed.

24. Claim 20 is objected to as being dependent upon rejected base claim, but would be allowable if rewritten in independent form including limitations of base and intervening claims.

Prior Art of Record

C. Eichenberger, W. Guggenbuhl, "On Charge Injection in Analog MOS Switches and Dummy Switch Compensation Techniques," *IEEE Transactions on Circuits and Systems*, vol. 37, pp. 256-264, 1990.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of advisory action. In no event, however, will statutory period for reply expire later than SIX MONTHS from date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

/Kee M Tung/
Supervisory Patent Examiner, Art Unit 2628